In the present embodiment, the generation of the crack "C" in the second dielectric layer 88 between the base member 12 and the first dielectric layer 85 is suppressed by the presence of the floating conductive layer 84, or the floating conductive layer 84 acts as a crack stopper for the second dielectric layer 88. Accordingly, the thickness of the entire circuit board can be reduced similarly to the first embodiment.

IN THE CLAIMS

Please rewrite claims 2 and 3 as follows:

2. (Once Amended) The circuit board as defined in claim 1, wherein the interconnect layer comprises a top interconnect layer on a top surface of the base member and a bottom interconnect layer on a bottom surface of the base member.

3. (Once Amended) The circuit board as defined in claim 2, wherein a volume of the top interconnect layer and a volume of the bottom interconnect layer are substantially equal.

REMARKS

The specification and claims 2-3 have been amended to overcome the objection to the disclosure and the rejection of claims 2-3 under 35 U.S.C. §112, second paragraph, respectively.

Claim 1 was rejected under 35 U.S.C. §102(b) as being anticipated by Tetsuo Mochizuki et al., Japanese Patent JP409181445A, hereafter referred to as Tetsuo.

It is an object of Tetsuo to prevent the printed circuit from peeling off the printed circuit board. In contrast, it is an object of the present invention to prevent the generation of a crack